Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **LO**
2. **COM**
3. **VCC**
4. **NC**
5. **NC**
6. **VS**
7. **VB**
8. **HO**
9. **NC**
10. **NC**
11. **VDD**
12. **HIN**
13. **SD**
14. **LIN**
15. **VSS**

**.098”**

**.120”**

**IR2110-REV2**

**DIE ID**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: .006” X .006”**

**Backside Potential:**

**Mask Ref: IR2110–REV2**

**APPROVED BY: DK DIE SIZE .098” X .120” DATE: 9/8/21**

**MFG: INT’L RECTIFIER THICKNESS .024” P/N: IRC2110C**

**DG 10.1.2**

#### Rev B, 7/19/02